Summary

Hall A – SoLID

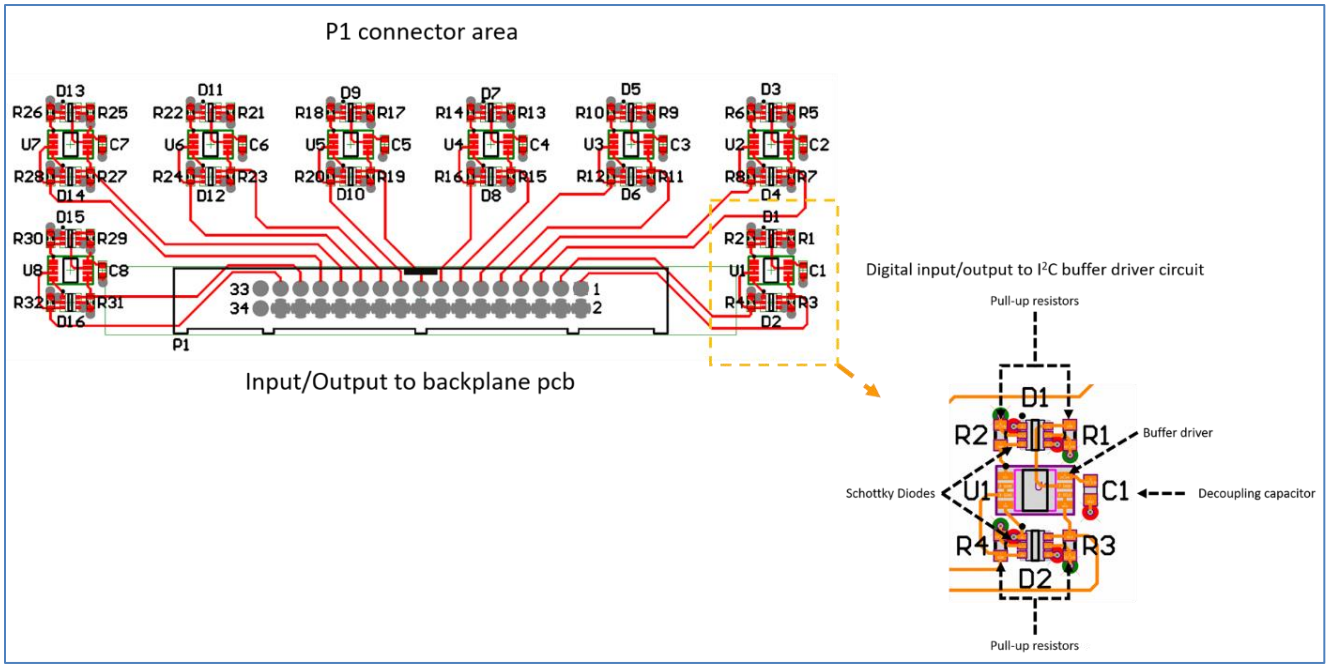
Mary Ann Antonioli, Pablo Campero, Mindy Leffel, Marc McMullen

- Generated flowchart to show the position control over JTV_3 – *LN_2 Bottom Fill Valve*
  - ✶ Flowchart shows automatic and manual control modes for the valve based on cryogenic condition (cooldown condition for the magnet shield)
  - ✶ No PID controls over this valve; it is either fully open or closed
- Updated list of electrical drawings to show status; 47% of drawings complete

Hall B – RICH-II

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Tyler Lemon

- Modifying sbRIO software for hardware interlock system
  - ✶ Software scaled up to read data from 48 sensors and calculate a rolling average
- Developing LabVIEW front panel for the hardware interlock system
- Developing Python program to assist configuring LabVIEW library for network shared variables and EPICS client
  - ✶ Program generates a CSV configuration file that can be read into LabVIEW so user doesn't have to manually enter configurations for all +200 variables
- Developing RMC PCB
  - ✶ Routing traces for output connectors, buffer drivers, and Schottky barrier diodes



Routed section of the RICH-II RMC; detailed view of the I/O connector area for channels 1-8

- Received the SHT-35 sensor PCB from the assembler
  - ✶ Performed a continuity check on one board

Hall B – SVT

Brian Eng

- Connected slow controls for SVT after cart was moved to Hall B

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Generated plots for long-term load test of HV supply cables and uploaded to DSG technical documentation webpage
- Developing LabVIEW front panel for hardware interlock system program
- Generating cable/instrumentation fabrication list for hardware interlock system development
- Researching cables and connectors to fabricate 50-pin Dsub extension cables for Keysight terminal blocks
- Fabrication of HV supply cables: 31 of 40 complete

EIC

Brian Eng

- Presented talk at JLab EIC and ECCE tracking meetings on current silicon model